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(54) **Name of Invention:** Method of Manufacturing
Semiconductor Devices

(57) **Summary**

Purpose: This invention is to provide a method for manufacturing semiconductor devices in which self-aligning contact holes can be formed for wiring layers that are effective with semiconductor devices having multi-layered wiring.

Constitution: One forms 1st barrier layers (16, 18) on a 1st conductive film (14) and patterns the barrier layers (16,

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18) and conductive film (14) in a batch to form 1st wiring layer pattern (22). Next, one forms a dielectric film (28). Then one forms 2nd conductive film (32) and 2nd barrier layers (34, 36) on the dielectric film (28) and patterns barrier layers (34, 36) and conductive film (32) together to a form 2nd wiring layer pattern (40). Next one forms a dielectric film (44). Then one forms a hole (51) reaching to the substrate (10) using at least one of the 1st barrier layers (16, 18) or 2nd barrier layers (34, 36) as etching barriers. Next, one forms sidewalls (54A~54C) on the sides of the opening (51). Then one forms a 3rd wiring layer pattern (56) in contact with the substrate (10) through the opening (51).

Scope of Patent Application

Application Item 1 A method of manufacturing a semiconductor device which is characterized by having -

- A process to form a 1st dielectric film on the surface of a semiconductor substrate,
- A process to form a 1st conductive film on this 1st dielectric film,
- A process to form a 1st barrier layer on this 1st conductive film,
- A process to pattern this 1st barrier layer and 1st conductive film together to form a 1st wiring layer pattern,
- A process to form a 2nd dielectric film on the upper surface of the above-noted substrate as to cover this 1st wiring layer pattern,
- A process to form a 2nd barrier layer on this 2nd conductive film,
- A process to form a 2nd wiring layer pattern by patterning this 2nd barrier layer and 2nd conductive film together,
- A process to form a 3rd dielectric film on the upper surface of the substrate so as to cover this 2nd wiring layer pattern,
- A process to form an opening through to the substrate, penetrating the 1st, 2nd and 3rd dielectric films while using at least one of the 1st and 2nd barrier layers as an etching barrier,

* [Bullets added by translator here and elsewhere in this document to facilitate reading.]

- A process to form a sidewall from a 4th dielectric film on the sides of this opening and
- A process to form a 3rd wiring pattern that is in contact with this substrate through this opening.

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Application Item 2 The method of manufacturing the semiconductor device described in Application Item 1, which is characterized by forming the above-noted 1st and 2nd barrier layers stacked in a lamination with a 1st material film consisting of a first material and a 2nd material film made of a 2nd material differing from that of the 1st material film.

Application Item 3 The method of manufacturing the semiconductor device described in Application Item 2, which is characterized by selecting for the above-noted 1st material a material that is dielectric and selecting for the above-noted 2nd material one that exhibits dielectric traits at least from being activated. Then, after forming the above-noted opening, doing a process to activate this 2nd material.

Application Item 4 The method of manufacturing the semiconductor device described in Application Item 3, which is characterized by this 1st material being selected from compound at least combining silicon and oxygen, and the above-noted 2nd material being selected from among silicon, hafnium, tantalum, zirconium, tungsten-silicide, molybdenum-silicide, hafnium silicide, tantalum-silicide and zirconium-silicide.

Application Item 5 A method of manufacturing semiconductor devices which is characterized by employing -

- A process to demarcate a 1st conductive-type element-forming region on the surface of the semiconductor substrate,
- A process to form a 1st dielectric film on the surface of the above-noted element-forming region,
- A process to form a 1st conductive film on this 1st dielectric film,
- A process to form a barrier layer on this 1st conductive film,
- A process to form a word-line pattern by patterning this 1st barrier layer and first conductive film in a batch,
- A process to form a 2nd source/drain region in the above-noted element-forming region, using the above-noted word-line pattern as a mask,
- A process to form a 2nd dielectric film on the surface of the substrate so as to cover the above-noted word-line pattern,
- A process to form a 1st opening on one side of this source/drain region through the above-noted 1st and 2nd dielectric films by using the above-noted 1st barrier

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- layer as an etching barrier,
- A process to form on the sides of this 1st opening a sidewall consisting of a 3rd dielectric film,
- A process to form a storage node electrode extending to one side of the above-noted source/drain region through this 1st opening,
- A process to form a 4th dielectric film on the surface of this storage node electrode,
- A process to form a 2nd conductive film on the above-noted 2nd dielectric film so as to cover this 4th dielectric film,
- A process to form a 2nd barrier layer on this 2nd conductive film,
- A process to form a cell-plate electrode pattern having a 2nd opening on the other upper side of this source/drain region by patterning the above-noted 2nd barrier layer and 2nd conductive film together,
- A process to form a 5th dielectric film on the above-noted 2nd dielectric film so as to cover this cell-plate electrode,
- A process to form a 3rd opening reaching to the other side of the above-noted source/drain region, going through the above-noted 1st, 2nd and 5th dielectric films and using one or the other of the above-noted 1st and 2nd barrier layers as an etching barrier,
- A process to form a 2nd sidewall consisting of a 6th dielectric film on the sides of this 3rd opening and
- A process to form a bit-line pattern contacting the other side of the above-noted source/drain region via this 3rd opening.

Application Item 6: The semiconductor device described in Application Item 5, which is characterized by the above-noted 1st and 2nd barrier layers being made laminated with a 1st material film of a first material and with a 2nd material film of a second material different from the first.

Application Item 7: The method of manufacturing the semiconductor device described in Application Item 6, which is characterized by selecting for the above-noted 1st material a material that has dielectric properties, selecting for the above-noted 2nd material one that exhibits dielectric traits at least upon being activated, and then, after forming the above-noted opening, doing a process to activate this 2nd material.

Application item 8: The method for manufacturing the semiconductor device described in Application Item 7 by

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which the above-noted 1st material is selected from among compounds that combine at least silicon and oxygen, and the above-noted 2nd material is selected from one or another of silicon, hafnium, tantalum, zirconium, tungsten-silicide, molybdenum-silicide, hafnium silicide, tantalum-silicide and zirconium-silicide.

Application Item 9: A method of manufacturing a semiconductor device which is characterized by having -

- A process to demarcate a 1st conductive-type element-forming region on the semiconductor substrate's surface,
- A process to form a 1st dielectric film on the surface of the above-noted element-forming region,
- A process to form a 1st conductive film on this 1st dielectric film,
- A process to form a barrier layer on this 1st conductive film,
- A process to form a word-line pattern by patterning this 1st barrier layer and first conductive film together,
- A process using the above-noted word-line pattern as a mask to form a 2nd conductive source/drain region in the above-noted element-forming region,
- A process to form a 2nd dielectric film on the surface of the substrate so as to cover the above-noted word-line pattern,
- A process to form a 1st opening that reaches to this source/drain region through the above-noted 1st and 2nd dielectric films by using the above-noted 1st barrier layer as an etching barrier,
- A process to form a first sidewall that is a 3rd dielectric film on the sides of this 1st opening,
- A process to form a second conductive film that contacts the other side of the above-noted source/drain region through the above-noted first opening,
- A process to form a 2nd barrier layer on this 2nd conductive film,
- A process that patterns this 2nd barrier layer and 2nd conductive film together to form a bit-line pattern contacting one side of the above-noted source/drain region,
- A process to form a 4th dielectric film so as to cover the above-noted bit-line pattern,
- A process to form a 2nd opening reaching to the other side of the above-noted source/drain region through the above-noted 1st, 2nd and 3rd dielectric films, using one or the other of the above-noted 1st and 2nd barrier

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- layers as an etching barrier,
- A process to form a 2nd sidewall consisting of a 5th dielectric film on the sides of the above-noted 2nd opening,
 - A process to form a storage node electrode reaching to one side of the above-noted source/drain region via the above-noted 2nd opening,
 - A process to form a 6th dielectric film on the surface of the above-noted storage node electrode and
 - A process to form a cell plate pattern on the above-noted 4th dielectric film so as to cover this 6th dielectric film.

Application Item 10: The semiconductor device described in Application item 9, which is characterized by the above-noted 1st and 2nd barrier layers being made laminated with the first being made of a first material and the second being made of a material differing from that of the first.

Application Item 11: A method of manufacturing the semiconductor device described in Application Item 10, which is characterized by selecting for the above-noted 1st material a material that has dielectric traits and selecting for the above-noted 2nd material one that exhibits dielectric traits at least from being activated, and, after forming the above-noted opening, doing a process to activate this 2nd material.

Application Item 12 The method for manufacturing the semiconductor device described in Application Item 11, which is characterized by the above-noted 1st material being selected from compounds at least combining silicon and oxygen, and the above-noted 2nd material being selected from among silicon, hafnium, tantalum, zirconium, tungsten-silicide, molybdenum-silicide, hafnium silicide, tantalum-silicide and zirconium-silicide, and the above-noted activation being an oxidation.

Detailed Explanation of Invention

0001 Field for Commercial Utilization: This invention bears on a method for manufacturing semiconductor devices, and in particular relates to forming contact holes that self-align with respect to wiring layer patterns.

0002 Usual Technology: With the miniaturization of semiconductor elements it has become difficult to get design leeway between the contact holes formed interposed with the internal wiring-layer patterns and the wiring layer patterns

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that adjoin these holes.

0003 Also, with the usual lithographic techniques it has been necessary to allow leeway for mask discrepancies between contact holes and wiring-layer patterns and even leeway for differences in hole diameters, even to the extent of impeding the miniaturizing of designs.

0004 To counter such problems, a so-called "self-aligning contact technique" has come to be developed by which sidewalls made of dielectric film are installed on the sides of the wiring layer pattern to insulate such wiring-layer patterns and contact holes from each other. The usual general "self-aligning contact technique" has been released in Patent Release Hei.2-30124. The "self-aligning technique" reported therein is summarized as follows.

0005 A polysilicon film and CVD oxidized silicon film are patterned together to get a pattern that includes an internal wiring layer (hereafter called a "gate") on a silicon substrate. Next, one forms a sidewall of CVD silicon oxide film on the sides of the pattern to include the gate. Then one forms sequentially on the substrate a silicon nitride film and polysilicon film on the pattern and gate and on the sidewall. This polysilicon film will become an etching barrier when an opening (hereafter, a "contact hole") is made later; i.e., it will become the sputtering layer. Next one forms on the polysilicon film a film of boron-phosphorus-silicon glass (hereafter "BPSG"). Then, using the polysilicon film as the etching barrier, one patterns the BPSG film by RIE [reactive ion etching] to get a contact hole reaching virtually through the patterns and gate to the substrate surface. Next, one uses the silicon nitride film as the etching barrier with the CDE method [Not defined -- Translator] to remove the silicon nitride film from this contact hole. Then, with the silicon nitride film as an oxidation barrier, one thermal-oxidizes the polysilicon film while making the BPSG film reflow. Next, with the BPSG film as the etching barrier, one uses the RIE method to remove the oxide film formed on the silicon nitride film and substrate surface from the contact hole. Then one forms an aluminum alloy film on the BPSG film, including the contact hole; and by patterning this aluminum alloy film one forms the internal wiring layer connected to the substrate. However, the above-described "self-aligning contact technique" is a method that can only be applied when using a wiring layer pattern consisting of one layer.

0006 Semiconductor devices are certain to be pressed hereafter to become further miniaturized and integrated.

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With this trend, the current internal wiring layers of semiconductor devices are moving from being just two layers of polysilicon and aluminum alloy to multi-layered wiring of three, four or more layers.

0007 Moreover, the fact is that at present no effective "self-aligning contact technique" has yet been developed for semiconductor devices having multiple wiring layers such as would, for example, contact the substrate through a 1st wiring layer from a 2nd wiring layer at the substrate.

0008 Matters the Invention Seeks to Resolve: This invention was worked out after considering the above-noted points; and its purpose is to provide a manufacturing method for semiconductor devices which can form contact holes that self-align with respect to wiring layers and so are effective with semiconductor devices having multiple wiring layers.

0009 Means to Resolve the Problems: This invention's method for manufacturing semiconductor devices is characterized by

- forming a 1st barrier layer on a 1st conductive film formed on a semiconductor substrate and patterning this 1st barrier layer and 1st conductive film together to form a 1st wiring layer pattern,
- next forming a 2nd dielectric film on the afore-noted substrate surface so as to cover the 1st wiring layer pattern,
- then forming a 2nd conductive film and 2nd barrier layer in sequence on this 2nd dielectric film,
- patterning a 2nd barrier layer and the above-noted 2nd conductive film together to form the 2nd wiring layer pattern,
- then forming a 3rd dielectric film on the surface of the afore-noted substrate so as to cover the 2nd pattern,
- next, using either one of the above 1st or 2nd barrier layers as an etching barrier, in making an opening through the 1st, 2nd and 3rd dielectric films to the afore-noted semiconductor substrate and forming a sidewall of a 4th dielectric film on the walls of this opening and
- then forming a 3rd wiring layer pattern in contact with the above-noted substrate through the above-noted opening.

0010 Also it is characterized by forming a 1st material film made of a first material and a 2nd material film of a

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second material differing from the first material and laminated with the above-noted 1st and 2nd barrier layers.

0011 Moreover, it is characterized by the material chosen for this first film having dielectric traits, the material chosen for the second material being activated to exhibit dielectric traits and by having a process to activate this second material.

0012 Effects With the above-noted method of manufacture, the 1st wiring layer pattern is formed by patterning the 1st barrier layer and 1st conductive film together. Also, the 2nd wiring layer pattern-separated electrically from the 1st wiring layer pattern by the 2nd dielectric film-is formed by patterning together the 2nd barrier layer and 2nd conductive film.

0013 With such a method, even if the etchant should come into contact with the 1st or 2nd wiring layer pattern when making the opening to the surface of the semiconductor substrate by etching the 2nd dielectric film, etc., these 1st and 2nd conductive films will be protected by the 1st and 2nd barrier layers. One can thus eliminate the problem of 1st and 2nd conductive films being etched away. Also, one has formed a sidewall with the 4th dielectric film on the walls of the opening.

0014 With this method, even if the opening exposes the 1st and 2nd conductive films, their exposed surfaces are covered by the 4th dielectric film, so that even when the 3rd wiring layer pattern is formed within the opening, the 1st and 2nd conductive films will not cause short circuits with the 3rd wiring layer pattern. Moreover, the 1st and 2nd barrier layers are respectively laminated with a film of a first material and a second film of a second material differing from the first material.

0015 With such an approach, any one of the films can be made resistant to a first etchant, while the other can be made resistant to a second different etchant, making it possible to strengthen the etching resistance overall of the 1st and 2nd barrier layers.

0016 Again, one selects for the above first material one having dielectric traits, and for the second material one that exhibits dielectric traits when activated. So, after forming the above-noted opening, one has this 2nd material activated.

0017 With such a method, even if one selects a material

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for the second material that is conductive, it can be made dielectric by activating it, and one can thus eliminate the problem of either the 1st or 2nd barrier layer short-circuiting the 3rd wiring layer.

0018 Materials that can work with this method are silicon, hafnium, tantalum, zirconium, tungsten-silicide, molybdenum-silicide, hafnium silicide, tantalum-silicide and zirconium-silicide. With these materials, one does the activation by oxidizing. When they are oxidized, their resistance values can be raised to equal those of dielectric materials.

0019 Application Examples Below, we will refer to the illustrations in explaining examples of applying this invention. In doing so, we use the same keying symbols for parts that are common to all the illustrations, and will avoid any duplicative explanations. Figures 1-14 are cross-sectional diagrams showing the processing order following the semiconductor manufacturing method for this invention's first application example.

0020 First, one thermal-oxidizes the surface of P-type silicon substrate 10 to get silicon oxide film 12 (SiO_2 - hereafter called a gate oxide film) some 200Å thick. Next, one uses the low-pressure CVD method (hereafter called an LPCVD method) to laminate polysilicon film 14 with a thickness of some 3000Å on gate oxide film 12. Then one uses vapor diffusion with POCl_3 as the source to diffuse phosphorus on polysilicon film 14, making it conductive (N type). Next one uses LPCVD to laminate silicon oxide film 16 about 3000Å thick on polysilicon film 14. Then one again uses LPCVD to laminate polysilicon film 18 about 200 Å thick on silicon oxide film 16 (Figure 1).

0021 Now one applies a photo-resist on polysilicon film 18. Then one etches this photo-resist by photolithography to form resist pattern 20 corresponding to the gate (word line). Next, using resist pattern 20 as a mask, one etches by RIE to etch sequentially polysilicon film 18, silicon oxide film 16 and N-type polysilicon film 14 to get 1st wiring layer pattern 22 that includes the gate pattern of N-type silicon film 14, silicon oxide film 16 and polysilicon film 18. Then, with wiring layer pattern 22 as a mask, one injects an N-type impurity such as arsenic into P-type substrate 10 to get N-type impurity layer 24 which will later become the transistor's source/drain (Figure 2).

0022 Now, after removing resist pattern 20, one uses LPCVD to sequentially form silicon oxide film 26 about 500Å thick

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and boron-phosphorus-silicon glass (BPSG) film 28 about 5000Å thick on substrate 10 so as to cover wiring-layer pattern 22. Silicon oxide film 26 and BPSG film 28 will function as interlayer dielectric films (Figure 3). In a nitrogen atmosphere one now causes BPSG film 28 to reflow at 850°C to flatten it (Figure 4).

0023 Next one uses LPCVD to laminate polysilicon film 30 about 1000Å thick on BPSG film 28. Then one deposits phosphorus on polysilicon film 30 to make it conductive (N-type). And, one uses DC magnetron sputtering to form tungsten-silicide (WSi_2) film 32 with a thickness of about 2000Å. Then one uses LPCVD to form on tungsten-silicide film 32 a silicon oxide film 34 about 3000Å thick and polysilicon film 36 about 500Å thick (Figure 5).

0024 Next, one applies a photo-resist to polysilicon film 36. Then one uses photolithography to etch this photo-resist and form resist pattern 38 matching the 2nd wiring layer. And, one uses resist pattern 38 as a mask to etch sequentially by RIE polysilicon film 36, silicon oxide film 34 and tungsten-silicide film 32. That gives one a 2nd wiring layer pattern that includes [1] a second wiring layer in which the main conductor is tungsten-silicide film 32, [2] silicon oxide film 34 and [3] a barrier layer of polysilicon film 36 (Figure 6).

0025 Next, after removing resist pattern 38, one uses LPCVD to form silicon oxide film 42 about 500Å thick and BPSG film 44 about 7000Å thick on BPSG film 28 so as to cover wiring layer pattern 40. Silicon oxide film 42 and BPSG film 44 function as interlayer insulating films (Fig. 7). Then one flattens BPSG film 44 by causing it to reflow in an 850°C nitrogen atmosphere (Figure 8).

0026 Now a photo-resist is applied to BPSG film 44 and this photo-resist is etched by photo-lithography to form resist pattern 46 with window 48 between the paired wiring patterns 40. At this point, window 48 is formed so as have a scope that includes the planned contact to substrate 10 and thus to be wider than the space between the patterns 40. As a result, window 48's sides 47 are positioned to be above wiring patterns 40 (Figure 9).

0027 Then, using resist pattern 46 as a mask, one etches-by RIE with an etchant such as CHF_3 ions-the BPSG film 44, silicon oxide film 42, BPSG film 28, silicon oxide film 26 and gate oxide film 12. That produces opening 50 reaching to substrate 10 (In the figure the N-type impurity layer 24) between 2nd wiring layer pattern 40 and first wiring layer

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pattern 22. This etching ends when polysilicon film 36 on 2nd wiring layer pattern 40 is etched, e.g., to some 400Å and when polysilicon film 18 on 1st wiring layer pattern 22 is etched, e.g., some 200Å. This is because, compared to the etching speed of BPSG, the etching speed of polysilicon is 1/60th as fast. After that resist pattern 46 is removed (Figure 10).

0028 Next, one does hydrogen combustion oxidation at 850°C to oxidize polysilicon films 14, 18, 20 and 30 where they are exposed in opening 50 and also the surface of tungsten-silicide film 32, changing them into oxides 14A, 18A, 30A, 36A and 32A. At this time, the surface of substrate 10 where it is exposed in opening 50 is also oxidized, forming silicon oxide film 52 about 150Å thick (Figure 11).

0029 Then one employs LPCVD to form silicon nitride film 54 about 2000Å thick on BPSG film 44 including the inside of opening 50 (Figure 12).

0030 Next, one does RIE etching of silicon nitride film 54 to form contact hole 51. At this point silicon nitride film 54 remains mainly on the upper sides of BPSG films 28 and 44 and of wiring layers 32 and 14. Also, during this etching oxides 18A and 26A sometimes are etched away. In such case, however, silicon oxide films 16 and 34 become etching stoppers, so that neither wiring layer 14 nor 32 will be etched (Figure 13).

0031 Now one uses LPCVD to form polysilicon film 56 about 3000Å thick with N-type conductivity due to its containing phosphorus. Next one uses photolithography to pattern polysilicon film 56 with the 3rd wiring layer pattern which contacts substrate 10 (N-type diffusion layer 24 in the figure) via contact hole 51 (Figure 14).

0032 When the method of manufacturing a semiconductor device is as in the above, one forms sidewall dielectric films 30A~30C on BPSG film 44 and wiring layer patterns 22 and 40, i.e., on the sides of opening 50 after having formed this opening 50 in BPSG film 44. So, sidewall dielectric films 30A~30C are not exposed to ions from the etching of BPSG films 28 and 44, making it easy to control the remaining sidewall dielectric films 30A~30C. Thus, good dielectric traits are obtained between the wiring layers, and one can especially raise the insulation level between wiring layers.

0033 Again, conductive polysilicon film 14 and tungsten-silicide 32 are patterned together with polysilicon films 18

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and 36, which will be barrier layers, and with oxide films 16 and 36, enabling one to prevent shorts among the wiring layers via polysilicon film 18.

0034 Furthermore, because polysilicon films 18 and 36 are removed from atop substrate 10 during patterning, where contact hole 51 will be formed, processes to remove polysilicon films 18 and 36 later from on substrate 10 are not needed. So, one can shorten the processing and improve productivity.

0035 Again, since polysilicon films 18 and 36 remain only at the top of the gate, the amount remaining is reduced. Due to that oxidizing them is easy. With polysilicon films 18 and 36 adequately oxidized, the problem of the wiring layers 56 formed in contact hole 51 shorting each other via these polysilicon films 18 and 36 is eliminated.

0036 Also, since one can form 2nd wiring layer pattern 40 even after reflowing BPSG film 28 that covers 1st wiring layer pattern 22, the above-noted manufacturing method is suited to devices having a multi-layered wiring structure.

0037 Furthermore, when silicon oxide film 34 and polysilicon film 36 which will become barrier layers are included in 2nd wiring layer pattern 40, as in the first application example, self-aligning contact holes 51 can be formed with respect to 1st wiring layer pattern 22 and 2nd wiring layer pattern 40. Figures 15~25 are cross-sectional diagrams showing the processing order in the manufacturing method for this invention's **second application example**. First with the fabrication method explained by referring to Figures 1~4, one gets the structure shown in Figure 15.

0038 Next, one uses LPCVD to laminate polysilicon film 30 about 1000Å thick on BPSG film 28. Then phosphorus is diffused over polysilicon film 30 to make it conductive (N type). Next one employs the DC magnetron sputtering method to form tungsten silicide (WSi_x) film 32 on polysilicon film 30 (Figure 16).

0039 Then one applies a photo-resist to tungsten silicide film 32 and uses photolithography to etch this photo resist and form resist pattern 38 corresponding to the 2nd wiring layer pattern. Now with resist pattern 38 as a mask, one sequentially etches tungsten silicide film 32 and N-type polysilicon film 30 by RIE to get 2nd wiring layer pattern 41 in which the main conductive part is tungsten silicide (Figure 17).

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0040 Next, after removing resist pattern 38, one uses LPCVD to form silicon oxide film 42 about 500Å thick and BPSG film 44 about 7000Å thick on BPSG film 28 and wiring layer pattern 41 (Figure 18). Then one flattens BPSG film 44 by causing it to reflow in a nitrogen atmosphere at 850°C (Figure 19).

0041 Now, applying a photo resist and using photolithography, one etches this photo resist to form resist pattern 46 with window 48 between wiring layer patterns 41. At this point, window 48 is made narrower than the width of the space between patterns 40 and so in a range to include the planned contact part on substrate 10. This results in the sides 47 of resist pattern 46 being positioned above wiring layer pattern 22 (Figure 20).

0042 Next, one uses resist pattern 46 as a mask to RIE etch BPSG film 44, silicon oxide film 42, BPSG film 28, silicon oxide film 26 and gate oxide film 12, for instance with CHF_3/CO ions as the etchant. That yields opening 50 reaching to substrate 10 (N-type impurity layer 24 in the figure) between wiring patterns 22. Compared to BPSG films 28 and 44, the etching speed of polysilicon film 18 is adequately slow at 1/60th or less. Due to this, the etching will end with polysilicon film 18 over 1st wiring layer pattern 22 being etched to about 200Å. Then the resist pattern is removed (Figure 21).

0043 Now one does hydrogen combustion oxidation at 850°C to oxidize the surfaces of polysilicon films 14 and 18 where they are exposed in opening 50 and change them into oxides 14A, 18A and 36A. At this point the exposed surface of substrate 10 in opening 50 also will oxidize, forming silicon oxide film 52 about 150Å thick (Figure 22).

0044 Then with LPCVD one forms silicon nitride (SiN_x) film some 2000Å thick on BPSG film 44 contained within opening 50 (Figure 23).

0045 Next, by the same method explained with reference to Figure 13, one uses RIE etching of silicon nitride film 54 to form contact hole 51. At this time silicon nitride film 54 remains mainly as sidewall dielectric films 54A and 54B on the upper sides of BPSG films 28 and 44 and wiring layer 14. Also, during this etching there are times when oxide 18A is not etched; and in such cases silicon oxide film 34 acts as a stopper so that oxide film 14 will not be etched (Figure 24).

0046 One then uses LPCVD to form polysilicon film 56 about

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3000Å thick containing phosphorus on BPSG film 44 included within contact hole 51. Next one uses photolithography to pattern polysilicon film 56 with the 3rd wiring layer pattern that contacts substrate 10 (N-type diffusion layer 24 in the figure) through contact hole 51 (Figure 25).

0047 With the semiconductor device manufactured by the above-noted method, contact hole 51 can be formed to self-adjust with respect to 1st wiring pattern 22. And, because sidewall dielectric films 54A and 54B are formed in this opening 50 after forming opening 50 in BPSG films 28 and 44 through to substrate 10, one can get the same kind of effects as with the first application example. Figure 26 is a cross-sectional diagram showing the final makeup of the semiconductor device made according to the fabrication method in this **third application example**.

0048 As Figure 26 shows, in semiconductor devices having three or more wiring layers it is possible to combine the methods described in the first and second application examples to form contact hole 51.

0049 In Figure 26, keying symbol 22, indicates a pattern that includes 1st wiring layer 14. Likewise, keying symbol 22, indicates a pattern containing 2nd wiring layer 14, ... symbol 22, indicates 4th wiring layer 14. Similarly, the 1st barrier layer consists of silicon oxide film 16, and polysilicon film 18, ... and the 4th barrier layer consists of silicon oxide film 16, and polysilicon film 18. Keying symbol 28, indicates interlayer dielectric film (BPSG, etc.) that insulates 1st wiring layer 14, and 2nd wiring layer 14, from each other; and, similarly, keying symbol 28, indicates an interlayer dielectric film that insulates 2nd wiring layer 14, and 3rd wiring layer 14, from each other, ... while keying symbol 28, indicates an interlayer dielectric film insulating 3rd wiring layer 14, and 4th wiring layer 14, from each other. Keying symbols 54A~54D indicate sidewall dielectric films (Si₃N₄, SiO₂, etc.) formed on the upper sides of interlayer dielectric films 28,~28, and wiring layers 14,~14.

0050 In the semiconductor device shown in Figure 26, contact hole 51 is deep. So, the barrier layer has a 2nd layer thicker than its 1st layer, a 3rd layer thicker than the 2nd and a 4th layer thicker than the 3rd layer—a desired progressive thickening. Due to that, for instance, even though the 4th barrier layer may be exposed for a longer time to the etchant, it can still endure. This may be achieved by setting the relative film thicknesses, for instance of polysilicon films 18,~18, as in the following.

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$$T_{18_1} < T_{18_2} < T_{18_3} < T_{18_4} \dots (1)$$

In equation (1), T_{18_1} indicates the thickness of polysilicon film 18₁, T_{18_2} the thickness of polysilicon film 18₂, T_{18_3} the thickness of polysilicon film 18₃, and T_{18_4} the thickness of polysilicon film 18₄. Next we will explain the **fourth application example** of this invention. Figure 27 is a plane diagram of the cell pattern of a dynamic RAM.

0052 As shown in Figure 27, source region 114₁ and drain region 114₂ are formed in element-forming region 101 where the silicon substrate's surface is exposed. Word lines (gate electrodes) WL are formed in element-forming region 101 between these two regions. Bit lines BL are connected electrically to drain region 114₂. The storage electrode is connected electrically to source region 114₁. In Figure 27 the storage electrode and cell-plate electrode are omitted.

0053 Figures 28~42 are cross-sectional diagrams of a dynamic RAM cell showing the processing sequence for the manufacturing method of the fourth application example of this invention. The cross sections are at the I-I line in Figure 27.

0054 First, one uses, for instance, the LOCOS [local oxidation of silicon] method to form silicon oxide film 102 (SiO_2 - hereafter, a field oxide film) on surface region 101 of P-type silicon substrate 100, defining element-forming region 101. Then, for instance by thermal oxidation, one forms silicon oxide film 102 (hereafter, a gate oxide film) about 150Å thick on element-forming region 101. Then, for instance by LPCVD, one forms polysilicon film 106 some 2000Å thick over the entire area of substrate 100. Next, with the vapor deposition method using POCl_3 as the source, one diffuses phosphorus on polysilicon film 106 to make this film conductive (N-type). Now one uses LPCVD to form silicon oxide film 108 about 3000Å thick on polysilicon film 106. After that one again uses LPCVD to form polysilicon film 110 about 100Å thick on polysilicon film 108 (Figure 28).

0055 Now one uses photolithography to form on polysilicon film 110 a resist pattern (not shown) corresponding to the word line pattern. Next, with the resist pattern as a mask, one uses RIE to etch polysilicon film 110, silicon oxide film 108 and N-type polysilicon film 106 in sequence. That forms word-line pattern 112 that includes the word line made

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up of N-type polysilicon film 106 and word-line pattern 112 to include a barrier layer consisting of silicon oxide film 108 and polysilicon film 110. Next, with word-line pattern 112 and field oxide film 102 as a mask, one injects into substrate 100 such N-type impurity ions as arsenic. That forms N-type impurity layer 114, consisting of the transistor's source and N-type impurity layer 114, that will be the drain. After that, the resist pattern (not shown) is removed (Figure 29).

0056 Next one uses LPCVD to form BPSG film 118 film and to form silicon oxide film 116 about 1000Å thick and BPSG film 118 about 4000Å thick on substrate 100 so as to cover word line pattern 112. Silicon oxide film 116 and BPSG film 118 function as interlayer insulating films. One flattens BPSG film 118 by causing it to reflow in a nitrogen atmosphere at 850°C (Figure 30).

0057 Next, one uses photolithography to form a resist pattern (not shown). This resist pattern has a window wider than the space between the two word line patterns and so a range that includes the planned contact of storage node electrode for contacting impurity layer 114, that will become the source. Then one uses the resist pattern as a mask in RIE etching with an etchant such as CHF_3/CO ions BPSG film 118, silicon oxide film 116 and gate oxide film 104. That yields opening 119 extending to impurity layer 114. Also, this etching is stopped by polysilicon film 110 at word-line pattern 112. That is due to polysilicon's etching rate being $1/60^{\text{th}}$ that of BPSG. After that the resist pattern (not shown) is removed (Figure 31).

0058 Now one does hydrogen combustion oxidation at 850°C to oxidize the surfaces of polysilicon films 106 and 110 where they are exposed in opening 119, thus yielding silicon oxide films 106A and 110A. At this time the surface of substrate 100 where it is exposed in opening 119 is also oxidized, forming silicon oxide film 122 about 200Å thick (Figure 32).

0059 Next, one uses LPCVD to form a silicon nitride film about 1000Å thick on BPSG film 118 within opening 119. Then one etches the silicon nitride film by RIE to form contact hole 120. At this point the silicon nitride film remains mainly on the sides of BPSG film 118 and of word line 106. That yields sidewall dielectric film 124 (Figure 33).

0060 Then with LPCVD one forms a polysilicon film about 1000Å thick on BPSG film 118 within contact hole 120. Next by gaseous diffusion one diffuses phosphorus onto the polysilicon film with POCl_3 as the source to make the

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polysilicon film conductive (N type). One then patterns the polysilicon film by photolithography, thereby getting storage node electrode 126 (Figure 34). And one oxidizes the surface of storage node electrode 126, e.g. by thermal oxidation, to form capacitor dielectric film 128 (Figure 35)

0061 One next uses LPCVD to form a polysilicon film of low resistance about 2000Å thick on BPSG film 118 to cover storage node electrode 126. This polysilicon film will become plate electrode 130. Now with LPCVD one forms silicon oxide film 132 about 1000Å thick on plate electrode 130, and then again uses LPCVD to form polysilicon film 134 about 400Å thick on silicon oxide film 132 (Figure 36).

0062 One next employs photolithography to form on polysilicon film 134 a resist pattern (not shown) corresponding to the opening so as to make the bit line at the plate electrode reach to the substrate. Then one uses the resist pattern as a mask to sequentially etch by RIE polysilicon film 134, silicon oxide film 132 and plate electrode (polysilicon film) 130. That forms plate electrode pattern 130 with its opening 136 for letting the bit line reach substrate 100. The width of slit 136 is made to be larger than the space between the word line patterns 112. Also plate electrode pattern 138 includes a barrier layer consisting of plate electrode 130, silicon oxide film 132 and polysilicon film 134. After that the resist pattern (not shown) is removed (Figure 37).

0063 Next one employs LPCVD to form silicon oxide film 140 about 1000Å thick and BPSG film 142 about 4000Å thick as interlayer dielectric films on BPSG film 118 so as to cover plate electrode pattern 138. And one then flattens BPSG film 142 by making it reflow at 850°C in a nitrogen atmosphere (Figure 38).

0064 Then one applies photolithography in applying a resist pattern (not shown) onto BPSG film 142. This resist pattern has a window wider than opening 136 and so in a range that includes the planned bit-line contact part which will be contacting impurity layer 114, which will be the drain. One now uses the resist pattern as a mask in RIE etching BPSG film 142, silicon oxide film 140, BPSG film 118, silicon oxide film 116 and gate oxide film 104, for instance with CHF₃/CO ions as the etchants. That yields opening 144 which extends to impurity layer 114. Also, this etching stops at polysilicon film 132 on plate electrode pattern 138 and at polysilicon film 110 on word-line pattern 112. This is because the etching rate of polysilicon is 1/60th that of BPSG. After that one removes

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the resist pattern (Figure 39).

0065 Next one does hydrogen combustion oxidation at 850°C to oxidize the surfaces of polysilicon films 106 (word line), 110, 130 (plate electrode) and 134 where they are exposed in opening 144, making them into oxides 106A, 110B, 130A and 134A. At this time the surface of substrate 100 will also be oxidized where it is exposed in opening 144, forming silicon oxide film 145 about 150Å thick (Figure 40).

0066 Now with LPCVD one forms silicon nitride film about 1000Å thick on BPSG film 142 contained in opening 144. One then etches the silicon nitride film by RIE to form contact hole 145. At this point the silicon nitride film remains mainly on the sides of BPSG films 118 and 142 and on the upper sides of word line 106 and plate electrode 130. That gives one sidewall dielectric film 148 (Figure 41).

0067 Again with LPCVD, one forms a phosphorus-bearing polysilicon film about 3000Å thick on BPSG film 142 in contact hole 145. One then uses photolithography to pattern the polysilicon film. This yields bit line 150 connected electrically to N-type impurity layer 114, via contact hole 145. With the above processes a dynamic RAM cell is formed with the flat plane pattern shown in Figure 27. Now we will explain the method for fabricating this invention's **fifth application example**. Figure 43 is a plane diagram of the dynamic RAM cell made using this fifth application example's fabrication method.

0068 As illustrated by Figure 43, the contact SNC for the storage node and source region 114, is installed in the region surrounded by bit line BL and word line WL. Also, element-forming region 101 is formed obliquely as seen from above so as to link with source region 114, on the opposite corner and bracket bit line BL. Bit line BL is connected electrically to drain region 114,. In Figure 43 the storage node electrode and cell-plate electrode are omitted.

0069 Figures 44(a)~(c) through Figures 54(a)~(c) are cross-sectional diagrams of the dynamic RAM cell of this invention's fourth application example and show the processing sequence in its method of fabrication. In the (a) diagrams they show, respectively, the cross sections of the a-a line, in the (b) diagrams the b-b line and in the (c) diagrams the c-c line in Figure 43.

0070 First, using the same methods explained in referring to Figures 27~29, one forms field oxide film 102 in the

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surface region of P-type silicon substrate 100, demarcating element-forming region 101. Then, after forming gate oxide film 104 on element-forming region 101, one forms word-line pattern 112 that includes a word line consisting of gate oxide film 104 on element-forming region 101 and a barrier layer consisting of silicon oxide film 108 and polysilicon film 110. One then forms N-type impurity layer 114 that will become the transistor's source and N-type impurity layer 114, that will become the drain [Figures 44(a)~(c)].

0071 Now, using the same method as was explained in reference to Figure 30, one forms silicon oxide film 116 and BPSG film 118 as interlayer dielectric films on substrate 100 so as to cover word-line pattern 112. Then one flattens BPSG film 118 by making it reflow [Figures 45(a)~(c)].

0072 Next one uses photolithography to form resist a pattern (not shown) on BPSG film 118. This resist pattern has a window wider than the distance between word line patterns 112 and thus with a range that includes a planned bit-line contact that will contact impurity layer 114, which will be the drain. Then one uses the resist pattern as a mask in RIE etching—with an etchant such as CHF_3/CO ions—BPSG film 118, silicon oxide film 116 and gate oxide film 104. That produces opening 144 through to impurity layer 114. This etching stops at polysilicon film 110 on word-line pattern 112 because the etching rate of polysilicon film is $1/60^{\text{th}}$ that of BPSG. After that, the resist pattern is removed [Figures 46(a)~(c)].

0073 Now one does hydrogen combustion oxidation at 850°C to oxidize the surfaces of polysilicon films 106 and 110 where they are exposed in opening 144 and thus get oxide films 106A and 110A. At this point, the surface of substrate 100 exposed within opening 144 is also oxidized, forming silicon oxide film 146 with a thickness of about 200\AA [Figures 47(a)~(c)].

0074 Next, one uses LPCVD to form a silicon nitride film about 1000\AA thick on BPSG film 118 within opening 144. Then one does RIE etching of the silicon nitride film to form contact hole 145. At this point the silicon nitride film remains mainly on the sides of BPSG film 118 and on the upper sides of word line 106. That gives one sidewalls 148 [Figures 48(a)~(c)].

0075 Then one employs LPCVD to form polysilicon film 152 about 3000\AA thick on BPSG film 118 in contact hole 145. Later, this polysilicon film will become a bit line. Next, one does vapor diffusion with POCl_3 as the source to diffuse

phosphorus on polysilicon film 152, making it conductive (N-type). Then, with LPCVD one forms silicon oxide film 152 about 1000Å thick on silicon oxide film 154. Again, with LPCVD one forms polysilicon film 156 some 250Å thick on silicon oxide film 154. After that, one uses photolithography to form a resist pattern (not shown) on polysilicon film 156. Then, with the resist pattern as a mask, one sequentially etches by RIE polysilicon film 156, silicon oxide film 154 and N-type polysilicon film 152. That forms bit-line pattern 158 that includes a barrier layer that will become a bit line consisting of N-type polysilicon film 152, silicon oxide film 152 and polysilicon film 154 [Figures 49(a)~(c)].

0076 Now by LPCVD one forms silicon oxide film 140 with a thickness of about 1000Å and BPSG film 142 with a thickness of about 6000Å as interlayer dielectric films on BPSG film 118 so as to cover bit-line pattern 158. Then one flattens BPSG film 142 by making it reflow in a nitrogen atmosphere at about 850°C [Figure 50(a)~(c)].

0077 Next, by photolithography one forms a resist pattern (not shown) on BPSG film 142. This pattern has a window wider than the space between the word-line patterns and so has the scope to contain the planned storage-node electrode's contact in impurity layer 114, that will become the source. Then one uses the resist pattern as a mask in sequentially etching by RIE, with an etchant such as CHF₃/CO ions, BPSG film 142, silicon oxide film 140, BPSG film 118, silicon oxide film 116 and gate oxide film 104. That makes opening 119 that goes through to impurity layer 114. The above-noted etching halts at polysilicon film 156 on bit-line pattern 158 and at polysilicon film 110 on word-line pattern 112. That is because polysilicon's etching rate is 1/60th that of BPSG. After that, one removes the resist pattern not in the figure [Figures 51(a)~(c)]. Also, Figure 55 is a plane diagram of the pattern in the process of Figures 49(a)~(c).

0078 Then at a temperature of 850°C one does hydrogen combustion oxidation to oxidize the surfaces of polysilicon films 106, 110 and 152 exposed in opening 121 to convert them to oxides 106A, 110A and 152A. Here the surface of substrate 100 is also oxidized where it is exposed in opening 119, forming silicon oxide film 122 about 200Å thick [Figures 52(a)~(c)].

0079 Then one uses LPCVD to form a silicon nitride film about 1000 Å thick on BPSG film 142. Next, one etches the silicon nitride film by RIE to form contact hole 120. The

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silicon nitride film now remains mainly on the sides of BPSG films 142 and 118 and on the upper sides of bit line 152 and word line 106. That creates sidewalls 124 [Figure 53(a)~(c)].

0080 Now on BPSG film 142 in contact hole 120 one forms a polysilicon film about 1000Å thick by LPCVD. Then with POCl₃ as the source for vapor diffusion of phosphorus on the polysilicon film, one makes that film conductive (N-type). Next, one patterns the polysilicon film by photolithography to get storage-node electrode 126. One then oxidizes the surface of storage-node electrode 126, such as by heating, to form capacitor dielectric film 128. Now one uses LPCVD to form a polysilicon film about 3000Å thick on BPSG film 142 and capacitor dielectric film 128 to make plate electrode 129 from this polysilicon film. With the above processes, the dynamic RAM's cell is formed with the plane pattern shown in Figure 43.

0081 This invention is not limited to the above-noted examples of its application, for, needless to say, its method of manufacture can be applied to parts other than memory cells' bit-line contacts or storage-node electrode contacts.

0082 Also, we used silicon oxide film and polysilicon as barrier films, but the polysilicon may be replaced by such other substances as hafnium, tantalum, zirconium, tungsten-silicide, molybdenum-silicide, hafnium-silicide, tantalum-silicide or zirconium-silicide. Just as with polysilicon, all such substances are oxidized and made dielectric by heat treatment at 700°C or more in an oxidizing atmosphere.

0083 Also, we made barrier layers by stacking silicon oxide film and polysilicon, which allowed us to bring to bear the etching resistance of either the polysilicon to the CHF₃/CO etchant or of the silicon oxide film to a chlorine etchant. Due to this, we got the effect of being able to strengthen overall the etching resistance of the barrier layers.

0084 Again, we used BPSG for the interlayer dielectric film; but such film may also be made up of phosphorus-silicate glass (PSG) or boron-silicate glass (BSG) whose qualities are all the same as BPSG. For instance, they can be made to reflow in oxidizing atmospheres by heating to 700°C or higher, and they give etching selectivity with Si, Hf, Ta, Zr, WSi₂, MoSi₂, HfSi₂, TaSi₂, or ZrSi₂. Moreover, we used silicon nitride film for sidewall dielectric films, but such films are not limited to nitride films so long as they are dielectric.

0085 Effectiveness of Invention: As described above, this invention provides a method of fabricating semiconductor devices that is effective with semiconductor devices having multiple wiring layers and that can form self-aligning contact holes.

Simple Explanation of Figures

Figure 1 is a cross-sectional diagram illustrating the first process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 2 is a cross-sectional diagram illustrating the second process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 3 is a cross-sectional diagram illustrating the third process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 4 is a cross-sectional diagram illustrating the fourth process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 5 is a cross-sectional diagram illustrating the fifth process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 6 is a cross-sectional diagram illustrating the sixth process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 7 is a cross-sectional diagram illustrating the seventh process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 8 is a cross-sectional diagram illustrating the eighth process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 9 is a cross-sectional diagram illustrating the ninth process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 10 is a cross-sectional diagram illustrating the 10th process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 11 is a cross-sectional diagram illustrating the 11th process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 12 is a cross-sectional diagram illustrating the 12th process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 13 is a cross-sectional diagram illustrating the 13th process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 14 is a cross-sectional diagram illustrating the 14th

process for manufacturing semiconductor devices with the first example of applying this invention.

Figure 15 is a cross-sectional diagram illustrating the first process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 16 is a cross-sectional diagram illustrating the second process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 17 is a cross-sectional diagram illustrating the third process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 18 is a cross-sectional diagram illustrating the fourth process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 19 is a cross-sectional diagram illustrating the fifth process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 20 is a cross-sectional diagram illustrating the sixth process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 21 is a cross-sectional diagram illustrating the seventh process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 22 is a cross-sectional diagram illustrating the eighth process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 23 is a cross-sectional diagram illustrating the ninth process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 24 is a cross-sectional diagram illustrating the 10th process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 25 is a cross-sectional diagram illustrating the 11th process for manufacturing semiconductor devices with the second example of applying this invention.

Figure 26 is a cross-sectional diagram of a semiconductor device manufactured with the method from the third example of applying this invention.

Figure 27 is a plane diagram of a dynamic RAM cell pattern from the method of manufacturing semiconductor devices per this invention's fourth application example.

Figure 28 is a cross-sectional diagram showing the first process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 29 is a cross-sectional diagram showing the second process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 30 is a cross-sectional diagram showing the third process in the method of manufacturing semiconductor devices

from this invention's fourth application example.

Figure 31 is a cross-sectional diagram showing the fourth process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 32 is a cross-sectional diagram showing the fifth process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 33 is a cross-sectional diagram showing the sixth process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 34 is a cross-sectional diagram showing the seventh process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 35 is a cross-sectional diagram showing the eighth process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 36 is a cross-sectional diagram showing the ninth process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 37 is a cross-sectional diagram showing the 10th process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 38 is a cross-sectional diagram showing the 11th process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 39 is a cross-sectional diagram showing the 12th process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 40 is a cross-sectional diagram showing the 13th process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 41 is a cross-sectional diagram showing the 14th process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 42 is a cross-sectional diagram showing the 15th process in the method of manufacturing semiconductor devices from this invention's fourth application example.

Figure 43 is a plane diagram of a dynamic RAM cell pattern fabricated by the manufacturing method for semiconductor devices under this invention's fifth application example.

Figure 44 is a cross-sectional diagram showing the first process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 45 is a cross-sectional diagram showing the second process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a)

being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 46 is a cross-sectional diagram showing the third process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 47 is a cross-sectional diagram showing the fourth process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 48 is a cross-sectional diagram showing the fifth process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 49 is a cross-sectional diagram showing the sixth process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 50 is a cross-sectional diagram showing the seventh process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 51 is a cross-sectional diagram showing the eighth process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 52 is a cross-sectional diagram showing the ninth process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 53 is a cross-sectional diagram showing the 10th process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b)

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the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 54 is a cross-sectional diagram showing the 11th process in the method of manufacturing semiconductor devices with the fifth example of applying this invention, with (a) being the cross section at the a-a line in figure 43, (b) the cross section at the b-b line and (c) the cross section at the c-c line.

Figure 55 is a plane diagram of the semiconductor device in the process shown in Figure 51.

Explanation of Keying Symbols

10	P-type silicon substrate
12	Gate oxide film
14	Polysilicon film with conductivity
16	Silicon oxide film
18	Polysilicon film
18A	Oxide
22	1 st wiring layer pattern
26	Silicon oxide film
28	BPSG film
30	Polysilicon film with conductivity
32	Tungsten-silicide film
34	Silicon oxide film
36	Polysilicon film
40, 41	2 nd wiring layer pattern
42	Silicon oxide film
44	BPSG film
50	Opening
51	Contact hole
54	Silicon nitride film
54A-54D	Sidewall dielectric film
56	Polysilicon film with conductivity
100	P-type silicon substrate
101	Element-forming region
102	Field oxide film
104	Gate oxide film
106	Polysilicon film with conductivity
108	Silicon oxide film
110	Polysilicon film
112	Word-line pattern
114 ₁	Source region
114 ₂	Drain region
116	Silicon oxide film
118	BPSG film
119	Opening
120	Contact hole
124	Sidewall dielectric film
126	Storage-node electrode

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128	Capacitor dielectric film
130	Plate electrode
132	Silicon oxide film
134	Polysilicon film
136	Opening
138	Plate electrode pattern
139	Plate electrode
140	Silicon oxide film
142	BPSG film
144	Opening
145	Contact hole
148	Sidewall dielectric film
150	Polysilicon film with conductivity (bit line)
152	Polysilicon film
154	Silicon oxide film
156	Polysilicon film
158	Bit-line pattern